Properties of Flip-Flops

By: Dr. A. D. Johnson   **Lab Assignment #9**
EECS: 1100 Digital Logic Design
The University of Toledo

1. Objectives

- gaining a close insight into the functioning and properties of basic static memory circuits,
- verifying the superior performance of the edge triggered JK-flip-flop over other kinds of JK-flip-flops regarding the multiple toggling and 1's catching properties,
- gaining insight into the static hazard property of some combinational logic circuits,
- getting familiar with characteristic tables and characteristic functions of the D-type flip-flops,
- getting familiar with state transition graphs of flip-flops,
- getting familiar with characteristic tables and characteristic functions of the T-type flip-flops,
- developing skills in the composition and testing of sequential logic circuits.

2. Prelab Assignment

2.1 EDGE-TRIGGERED JK-FLIP-FLOP

2.1.1 Using the present stable state variables J, K, and Q, and the next stable state variable Q+, prepare a *characteristic table* of the edge-triggered JK-flip-flop and show it as Table T2.1-1.

2.1.2 Compare the characteristic table T2.1-1 to the truth table T2.3-1 of the Lab Assignment #8, and state their common features and their differences. Could the difference be attributed to the differing transparency properties of the edge-triggered JK-flip-flop and the level-controlled JK-flip-flop circuits?

2.1.3 Using the prepared characteristic table T2.2-1 and the Karnaugh map minimization method, derive a minimized expression of the characteristic equation of the edge-triggered JK-flip-flop. Show the derived equation as equation (2.2-1).

2.1.4 Based on the prepared characteristic table T2.2-1, draw a graphical representation of the state transition graph (state diagram) of the edge-triggered JK-flip-flop, and show it as Figure 2.1-1.

2.1.5 Prepare a computer generated drawing of the logic circuit of Figure A.2-1 and show it as Figure 2.1-2(a).

Hint#1 Note that the NOR and AND gates in Figure A.2-1 create a combinational circuit with a static 0-hazard, which establishes conditions for the 1's catching to take place. To that effect, the static 0-hazard circuit will deliver a positive glitch to the input of the OR gate on every positive edge of the signal Q_A; the glitch will be transferred to J input of the JK-flip-flop while Q_B is at *logical 0*. The buffer-connected AND gate increases the time delay of the signal generated by the NOR gate to make the duration of the glitch longer.

2.1.6 Design a physical layout of the logic circuit shown as Figure 2.1-2(a). Prepare a computer generated drawing of the layout and show it as Figure 2.1-2(b). Provide the IC package pinouts on both drawings of Figure 2.1-2.
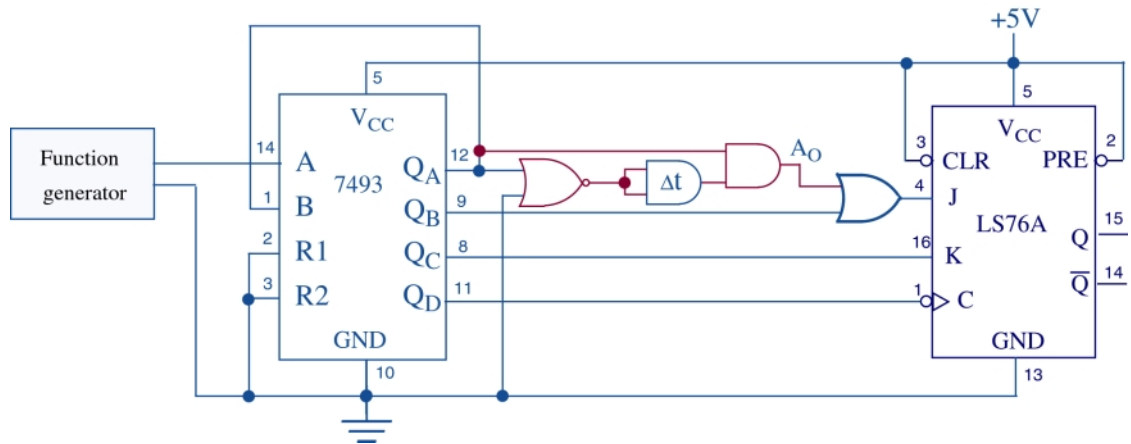

Figure A.2-1 A circuit for experimenting with the Edge-Triggered JK-flip-flop.

2.1.7 Data sheets of the 74LS76A dual negative-edge triggered JK-flip-flop are available in the TTL Data Book.

Hint#2: Pinouts (pin numbers) are available in Figure 2.5 of the course text book, pp.107-109, and in the TTL Data Book.

2.2 NEGATIVE EDGE TRIGGERED D-FLIP-FLOP

2.2.1 Using the present state variables D and Q, and the next state variable Q^+, prepare a *characteristic table* of the D-flip-flop and show it as Table T2.2-1.

2.2.2 Using the prepared characteristic table T2.2-1 and the Karnaugh map minimization method, derive a minimized expression of the characteristic equation of the D-flip-flop and show it as equation (2.2-1).

2.2.3 Based on the prepared characteristic table T2.2-1, derive a graphical representation of the state transition graph (state diagram) of the edge-triggered D-flip-flop, and show it as Figure 2.2-1.

2.2.4 Design a logic circuit which implements a negative edge-triggered D-flip-flop by "gating" the D input to the inputs of a JK-flip-flop circuit. Show a graphical representation of the D-flip-flop circuit as Figure 2.2-2(a).

Hint#3 Consider using an inverter.

2.2.5 Using integrated circuit components listed in section 3.2, design a physical layout of the logic circuit shown in Figure 2.2-2(a). Show a computer generated drawing of the designed layout as Figure 2.2-2(b). Provide IC package pinouts in all drawings of Figure 2.2-2.

Hint#4 Pinouts are available in the data sheets of the 74LS76A in the TTL Data Book.

2.3 T-FLIP-FLOP

2.3.1 Using the present state variables T and Q, and the next state variable Q^+, prepare a *characteristic table* of the T-flip-flop and show it as Table T2.3-1.

2.3.2 Using the prepared characteristic table T2.3-1 and the Karnaugh map minimization method, derive a minimized expression of the characteristic equation of the T-flip-flop and show it as equation (2.3-1).

2.3.3 Based on the prepared characteristic table T2.3-1, derive a graphical representation of the state transition graph (state diagram) of the edge-triggered T-flip-flop, and show it as Figure 2.3-1.

2.3.4 Design a logic circuit which implements an edge-triggered T-flip-flop by "gating" the T input to the inputs of a JK-flip-flop circuit. Show a computer generated graphical representation of the T-flip-flop circuit as Figure 2.3-2(a).

Hint#5 Compare the characteristic tables of the T-flip-flop and the JK-flip-flop to find out how to connect the T-input to inputs J and K.

2.3.5 Design a physical layout of the logic circuit shown in Figure 2.3-2(a). Show a computer generated drawing of the designed layout as Figure 2.3-2(b). Provide IC package pinouts in all drawings of Figure 2.3-2.

3. Lab Equipment and Circuit Components

3.1 EQUIPMENT

Equipment to be used includes:

- Protoboards: Global PB-104, or PB-105,
- Agilent E3631A DC power supply,
- Function generator: Agilent 33120A,
- Mixed-Signal oscilloscope Agilent 54645D,
- Dell GxaEM computer system.

3.2 LOGIC GATE AND CIRCUIT COMPONENTS
- integrated circuit 7402, quad 2-input NOR gates (1)
- integrated circuit 7404, hex inverters (1)
- integrated circuit 7408, quad 2-input AND gates (1)
- integrated circuit 7432, quad 2-input OR gates (1)
- integrated circuit 74LS76A, dual negative-edge triggered JK-flip-flop (1)
- integrated circuit 7493, 4-bit ripple counter (1)

4. Lab Experiment

4.1 EXPERIMENT WITH THE EDGE-TRIGGERED JK-FLIP-FLOP

4.1.1 Using the prepared physical layout of Figure 2.1-2(b), build on the protoboard the circuit shown in Figure A.2-1.

4.1.2 Connect the digital channels D0 through D7 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.3.1:

- digital channel D0: to the output of the Agilent 33120A function generator,
- digital channel D1: to the flip-flop input signal J,
- digital channel D2: to the flip-flop input signal K,
- digital channel D3: to the flip-flop clock signal C,
- digital channel D4: to the flip-flop output Q,
- digital channel D5: to the flip-flop output $\overline{Q}$.
- digital channel D6: to the output of the 2-input AND gate A_O ,
- digital channel D7: to and to ripple counter's output Q_A .

Establish a ground connection. Turn on digital channels D0 through D7, and rename the channels D0 through D7 as A, J, K, C, Q, QB, AO, and QA respectively.

4.1.3 Adjust the frequency of the Agilent 33120A function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 00 on channels D1 through D2. Hit the key Single on the Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 00 on channels D1 through D2 is positioned at the left end of the screen, and that the whole screen shows ten percent more than two periods of the clock signal C.

4.1.4 Investigate the waveforms obtained under 4.1.3, looking for the evidence of errors caused by the *multiple toggling* or *1's catching* properties of some flip-flops. Could you observe occurrence of any of those? Based on your observations: Is the Edge-Triggered JK-flip-flop a reliable memory element?

4.1.5 Save the Screen Image of the correct waveforms of the digital channels D0 through D6 to a file named L9_415.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.1.6 Create the circuit of Figure A.4-1 by making necessary modifications to the circuit of Figure A.2-1. Leave the connections of the digital channels D0 through D5 of the Agilent 54645D oscilloscope unchanged, and remove the connections to D6 and D7. Repeat the actions specified under 4.1.3.
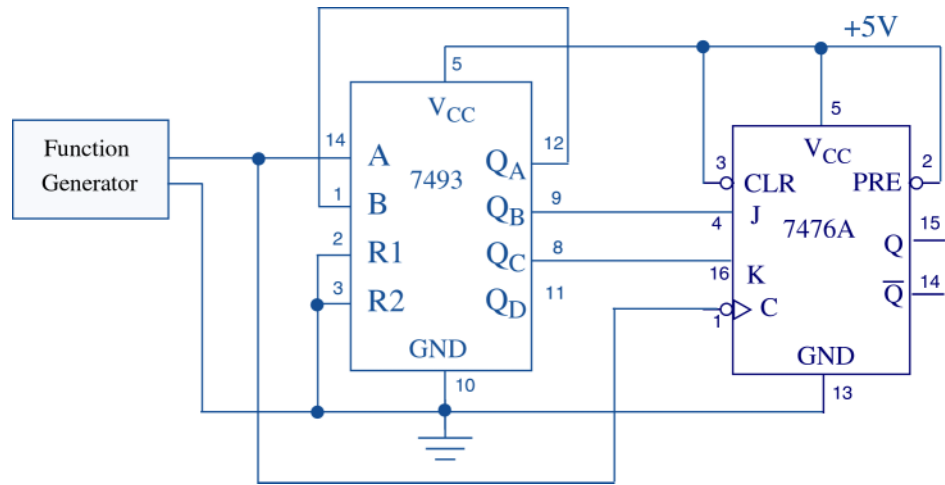
Figure A.4-1 A circuit for experimenting with the Edge-Triggered JK flip-flop.

4.1.7 Save the Screen Image of the correct waveforms of the digital channels D0 through D6 to a file named L9_415.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.1.8 Observe the waveforms and compare them with those obtained in the circuit of Figure A.2-1. State the differences that you can observe. Explain what causes the differences.

Hint#7 The ratio of the clock signal (control signal C) frequency to the frequencies of the input signals J and K is smaller than one in the circuit of Figure A.2-1, while it is greater than one in the circuit of Figure A.4-1. Consider how this affects the selection of input signal combinations at which the triggering of the flip-flop takes place.

4.2 EDGE-TRIGGERED D-FLIP-FLOP

4.2.1 Using as a reference the prepared physical circuit diagram from Figure 2.2-2(b), build on the protoboard an implementation of the circuit of Figure A-4.2.
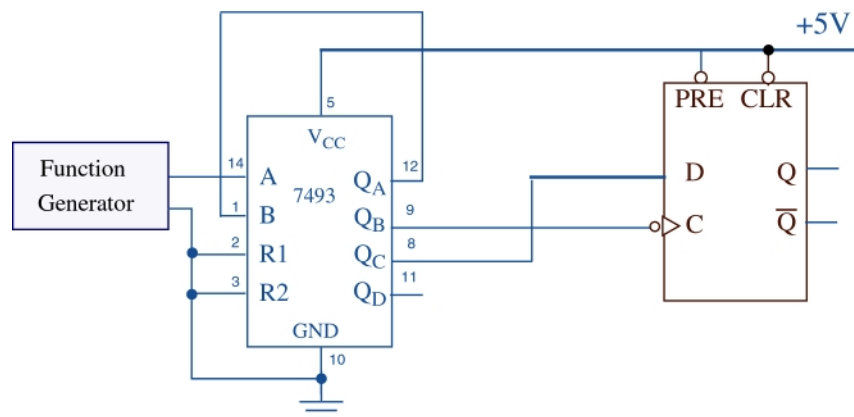

Figure A.4-2 Circuit for experimenting with the Edge-Triggered D-flip-flop.

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4.2.2 Connect the digital channels D0 through D4 of the Mixed signal oscilloscope Agilent 54645D to the circuit shown in Figure A-4.2:

- digital channel D0: to the output of the function generator,

- digital channel D1: to the flip-flop input signal D,

- digital channel D2: to the flip-flop control signal (clock) input C,

- digital channel D3: to the flip-flop output signal Q,

- digital channel D4: to the flip-flop output signal QB,

Establish a ground connection. Turn on digital channels D0 through D4, and rename the channels D0 through D4 as A, D, C, Q and QB respectively.

4.2.3 Adjust the frequency of the function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 00 on channels D1 and D2. Hit the key Single on the Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 00 on channels D1 through D2 is positioned at the left end of the screen, and that the whole screen shows ten percent more than two periods of the signal at the input D. Compare the obtained waveforms with the contents of Table T2.2-1. In case of a discrepancy remove the cause and repeat the experiment.

4.2.4 Save the Screen Image of the correct waveforms of channels D0 through D4 to a file named L9_424.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.2.5 Disconnect the input C from the output Q_B of the 7493 pulse source and connect it to the output Q_A of the 7493. Obtain a new set of waveforms in the same way as in Section 4.2.3. Observe the obtained waveforms. Compare the new set of waveforms with the one obtained in Section 4.2.3. Explain the cause of the difference in the time moment when the output of the D-flip-flop changes

Hint#6 Consider the time delay of the signal at the input D with respect to the time of the negative edge of the signal at C. Was it greater in the circuit of the experiment performed under 4.2.3, or 4.2.5? Zoom in at the moment of the negative edge of the clock signal and determine the actual timing sequences at D and C. Consider the influence of the setup time of the flip-flop.

4.2-6 Save the Screen Image of the correct waveforms of channels D0 through D4 to a file named L9_42.6.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.3 EDGE-TRIGGERED T-FLIP-FLOP

4.3.1 Using as a reference the prepared physical circuit diagram of Figure 2-3(b), build on the protoboard the test circuit shown in Figure A.4-3.
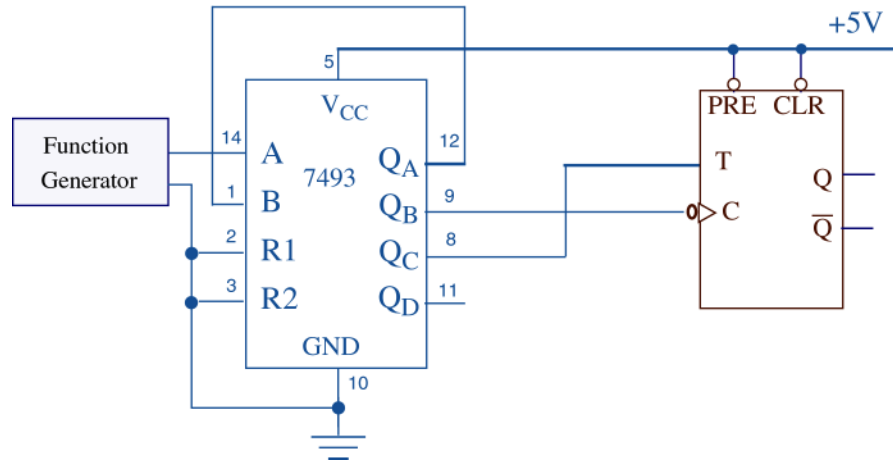

Figure A.4-3 Circuit for experimenting with the Edge-Triggered T-flip-flop.

4.3.2 Connect the logic channels D0 through D4 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit shown in Figure A.4-3:

- digital channel D0: to the output of the Agilent 33120A function generator,

- digital channel D1: to the flip-flop input signal T,

- digital channel D2: to the flip-flop control signal C,

- digital channel D3: to the flip-flop output signal Q,

- digital channel D4: to the flip-flop output signal QB.

Establish a ground connection. Turn on digital channels D0 through D4, and rename the channels D0 through D4 as A, T, C, Q and QB respectively.

4.3.3 Repeat the steps of Section 4.2.3. Investigate the obtained waveforms and compare them with the contents of Table T2.3-1. In case of a discrepancy remove the cause and repeat the experiment.

4.3.4 Save the Screen Image of the correct waveforms of channels D0 through D4 to a file named L9_434.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.4 TRANSFER OF CAPTURED WAVEFORMS.

Transfer (ftp) the files L9_*.tif from the Dell GxaEM computer system to your personal College of Engineering computer account.

5. Lab Report

To be considered complete, the lab report must contain the following,

1. Cover sheet - Lab style, filled out,

2. The truth tables prepared under 2.1 through 2.3.

3. The characteristic functions of flip-flops derived under 2.1 through 2.3.

4. The logical and physical circuit diagrams prepared under 2.1 through 2.3.

5. The waveforms obtained in experiments 4.1 through 4.3.

6. Answers to all questions asked in conjunction with experiments 4.1 through 4.3.

7. A report on items not already included under 1. through 6. above, which includes:

   - a discussion of the insights gained through the conducted experiments,

   - textual description and graphical/ tabular illustration of the design procedure(s),

   - description of implemented testing procedures,

   - conclusions reached as a result of performing the lab experiment,

   - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.